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Importance of Thermophysical Properties of Thin Films in Ultra-Large-Scale Integrated Circuits and Beyond[1]

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Ultralarge-scale integrated circuits (ULSICs) are fabricated in a single crystal of silicon using submicron device structures arrayed in two dimensions, which are interconnected in the third dimension with multilevel metallizations. The latter use several alternating layers of metal and dielectric films. Currently, four-level metallizations are used in large volume ULSIC manufacturing. As the technologies advance in ULSICs and beyond, four-level metallizations are expected to increase to six-level and higher. In three-dimensional ICs (3-D ICs) and ultraperformance ICs (UPICs), in which active devices are also fabricated in the third dimension in addition to the interconnects, the total number of semiconductor, dielectric, and metal films increases significantly. The thermophysical properties of all of these films play an ever-increasing role in the overall yield, reliability, and chip size of the ICs. The thermophysical properties considered in this paper are the thermal conductivity κ and the stress σ and its variations on thermal cycling, of the SiO_2 films only. Data for these parameters are shown, with comments on their impact on the reliability of the ICs, and the role of Umklapp and point defect scattering mechanisms on the κ of thin films is discussed. The thermophysical properties not only are important in the current ULSICs for enhanced performance and reliability, but are even more crucial for the design and manufacturing of the next generation ICs like 3-D ICs and UPICs.

KEY WORDS: *electromigration lifetime; integrated circuits; reliability;* SiO_2 films; stresses thermal conductivity.

1. INTRODUCTION

Currently available ultralarge-scale integrated circuits (ULSICs) have about 5–10 million transistors arrayed as densely as allowed by the design

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rules in two dimensions on a single crystal of silicon, which are interconnected by four-level multilevel metallizations [1]. The key objectives are to obtain the smallest IC chip, with maximum performance, reliability, and yield. The multilevel metallizations use alternating layers of aluminum-based alloys having under- and cap layers of refractory metals, and SiO_2-based interlayer-dielectric (ILD) films [2]. The film thicknesses can range from a few hundred to several thousand angstroms. The thermophysical properties such as thermal conductivity κ and stress σ of these films are important for the reliability of the ULSICs. While the κ and σ of both the metal and the ILDs need to be considered, only the data for SiO_2 ILDs will be presented in this paper. The κ of thin SiO_2 films is lower than its value κ_B for bulk quartz. The latter has been widely used for the thermal modeling of the ICs, which will give erroneous values for the electromigration lifetime t_{50} of the interconnects. The stress σ of the ILDs varies on thermal cycling, and its value and type, i.e., whether it is compressive or tensile, have an effect on the t_{50}. Knowing and controlling the κ and σ of the ILDs can enhance the performance and the reliability of the ICs.

2. THERMAL CONDUCTIVITY

2.1. Variation with Film Thickness

The thermal conductivity κ of SiO_2 films varies with their film thickness and, also, with their method of deposition, growth, and composition [3]. The measurement technique for obtaining κ and the details of the processes used for producing the various SiO_2 films have been given earlier [3]. Figure 1 shows the measured values of κ for these SiO_2 films vs their film thicknesses t_{ox}. The various processes used for the deposition of the SiO_2 films were thermal growth (thermal), plasma enhanced CVD for undoped (PTEOS and SiH_4), phosphorus-doped (PSG), boron + phosphorus-doped (BPSG), and a nonplasma O_3-assisted CVD of TEOS (O_3-TEOS) for undoped films. The thermal conductivity of bulk fused quartz κ_B is also shown in Fig. 1, which is independent of "film thickness" and its value in the units chosen is 14 $mW \cdot cm^{-1} \cdot {}^{\circ}C^{-1}$. As can be seen from the data in Fig. 1, the κ values of the various SiO_2 films are lower than κ_B, they decrease with decreasing film thicknesses t_{ox}, and they vary with the process used for their deposition. When the κ values were plotted for the various SiO_2 films vs their respective $1/t_{ox}^{1/2}$, a linear behavior was observed for all the films. This is shown in Fig. 2 for the thermal, PTEOS, and the annealed PTEOS-a films only. Such a linear behavior is predicted by the model of Savvides and Goldsmid [4].

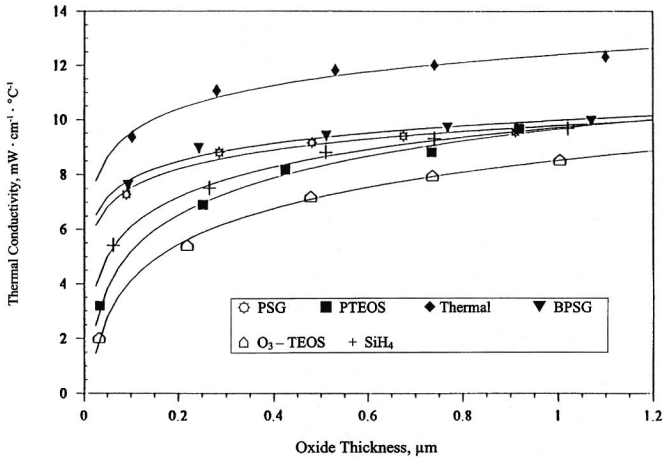

Fig. 1. Thermal conductivity of PSG, PTEOS, thermal, BPSG, SiH_4, O_3-TEOS oxides at 22°C vs oxide thickness.

2.2. Annealing Effects and Diagnostics for Film Quality

As mentioned in the previous Section 2.1, the experimental κ data of various types of SiO_2 films vs $1/t_{ox}^{1/2}$ fit their respective straight lines. When they are extrapolated to the origin at $1/t_{ox}^{1/2} = 0$, the intercept gives κ_o, which is the "extrapolated bulk thermal conductivity," for each film. The details of the data and analyses are given in Ref. 3. However, Fig. 2 shows that the κ_o for the annealed PTEOS film is greater than that for the

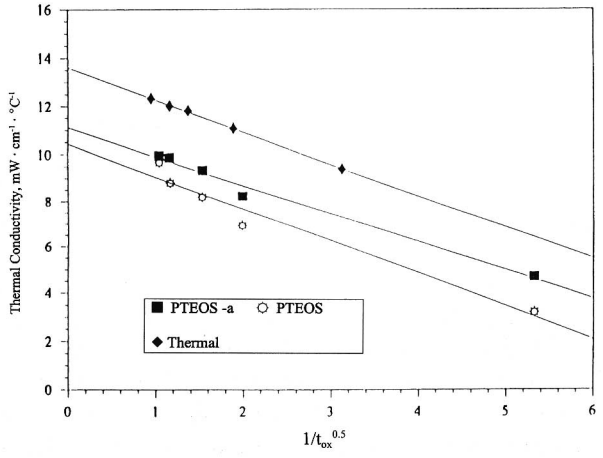

Fig. 2. Thermal conductivity of as-deposited, annealed PTEOS and thermal oxides at 22°C vs $1/t_{ox}^{1/2}$.

as-deposited PTEOS film. This is because of the densification of the PTEOS film due to annealing. It was also observed that the κ_o of the thermally grown SiO_2 film is the highest ($13.6\,mW \cdot cm^{-1} \cdot °C^{-1}$) of all the SiO_2 films studied and that it was closest to the bulk quartz value $\kappa_B = 14\,mW \cdot cm^{-1} \cdot °C^{-1}$. Thus, the experimentally measured κ_o of a film can be used as a diagnostic for the SiO_2 film quality and for the reproducibility of the process used for manufacturing the film.

2.3. Diagnostics for Adhesion

The number of films used in the manufacturing of ULSICs is ever increasing and is expected to continue to increase as the technologies advance. The adhesion of each film, e.g., photoresist, ILDs and multilevel metal films, during the manufacturing processes, and in the finished ULSIC product, is absolutely crucial for device yield and reliability. No quantitative technique to characterize and monitor adhesion, in particular in the submicron geometries used in ULSIC manufacturing, had even been proposed much less used in practice, until recently [5]. The slope, s, of the straight line in Fig. 2 is related to the mean free relaxation times for Umklapp phonon scattering, τ_U, and for phonon scattering by point defects in the material of the film, τ_{PD}. The τ_{PD} is related to its bulk and surface scattering components, the latter being dependent on the adhesion of the film to the surface. A model was proposed [5] which gives s as the parameter to characterize adhesion quantitatively for a given film and its manufacturing process. The value of s decreases as the film adhesion gets better. As an example, Fig. 2 shows that the slope s of the annealed PTEOS film, PTEOS-a, is 1.22, which is lower than 1.40 for the same as-deposited PTEOS film before annealing. This is of course due to the improvement of adhesion of the PTEOS film on annealing. Analyses similar to that given in Ref. 5 need to be extended to characterize other films used in ULSIC manufacturing.

2.4. Impact on Reliability

Two aspects of reliability shall be addressed here, *viz*, electromigration lifetime, t_{50}, of aluminum-based interconnects (AlX) and adhesion of films. The t_{50} depends exponentially on, and decreases with, the temperature of AlX interconnects [6] used in the multilevel metallizations of ULSICs. The increase in temperature during the use and/or accelerated testing of the ULSICs is inversely proportional to the thermal conductivity of the ILDs, and it is directly proportional to the interconnect metal resistivity and thickness, the thickness of the ILDs, and the square of the current density

being used in the interconnects [7]. Thus for a given structure of multilevel metallizations and the use conditions in the ULSICs, the lower the thermal conductivity of the ILD, the lower would be the t_{50}. When the bulk thermal conductivity value κ_B is used in the thermal modeling, the t_{50} value calculated will be higher than the actual value of t_{50}, which will be obtained with the true values of κ corresponding to the thicknesses of the ILDs in the ULSIC. Therefore, a user of the ULSIC can have misleading information on its reliability. To enhance the reliability, proper attention needs to be paid to the thermal conductivity and the other parameters of the ULSIC films.

The adhesion of the various films needs to be good during and after the processing of the ULSICs. The measurement of the slope s defined in Section 2.3, using microminiature test devices having submicron geometries such as those of the ULSICs, provides the quantitative characterization of adhesion during and after normal and accelerated testing of there ULSICs. Thus, for a given film interface, a minimum value of s and maintaining its constant value, will give the highest reliability.

3. STRESSES

Stresses in all of the films used in ULSICs are important for device yield, reliability, and performance. However, the stress behavior of only SiO_2 ILDs are discussed in this paper. For details, see Refs. 8 and 9.

3.1. Variation with Post-Metal-1 Thermal Recycling

Post-metal-1 thermal recycling is defined as the temperature range through which the ULSIC wafers are subjected; the maximum temperature should not exceed about 450 °C. This is to prevent the interaction of AlX metallizations with Si. As shown in Ref. 8, an ILD having an initial small compressive stress, ends up with a high tensile stress after the post-metal-1 thermal recycling. A simplified explanation for such a behavior is that the "SiO_4" tetrahedra in the ILD do not acquire sufficient energy in this thermal regime to reconfigure themselves.

3.2. Variation with Pre-Metal-1 Thermal Recycling

Pre-metal-1 thermal recycling is defined as the temperature range through which the ULSIC wafers are subjected in excess of 450 °C, usually up to about 950 °C. Higher temperatures can be reached in this recycling, because no metal has been deposited yet on the ULSIC wafers. Again, as shown in Ref. 8, an ILD having an initial small compressive stress, ends up

with a slightly higher compressive stress after the pre-metal-1 thermal recycling. A simplified explanation for such a behavior is that the "SiO_4" tetrahedra in the ILD do acquire sufficient energy in this thermal regime to reconfigure themselves.

3.3. Stress Type and Reliability

It has been shown [9] that the stress type in the ILD has a significant effect on the electromigration lifetime, t_{50}, of AlX interconnects. The effect of the stress type, i.e., whether it is compressive or tensile, manifests itself in the residual resistivity of the AlX. Figure 3 shows the variation of AlX resistance vs temperature for three cases: one with tensile ILD, second with compressive ILD, and third without any ILD, i.e., unpassivated [9]. The residual resistivity behavior regime is observed at temperatures $<40°$ K. The value of the residual resistivity is observed to be highest for an AlX interconnect with an ILD having a compressive stress, it is lower with an ILD having a tensile stress, and it is lowest when no ILD is used, i.e., when the AlX interconnect is unpassivated. A model to explain this behavior has been given earlier [10]. The significance of all this is that all the interconnects being currently used in the ULSICs are AlX-based, and they are all passivated with SiO_2-based ILDs. It has been shown [9, 10] that the t_{50} of AlX interconnects is approximately 100% higher with ILDs having tensile stress as compared to those having compressive stress. To get the highest t_{50} in a given multilevel metallization structure of ULSIC, and achieve the highest reliability, further work is necessary to optimize the parameters of the stress values, types, thicknesses, processes, etc. A quantitative electrical characterization technique to monitor the quality and the

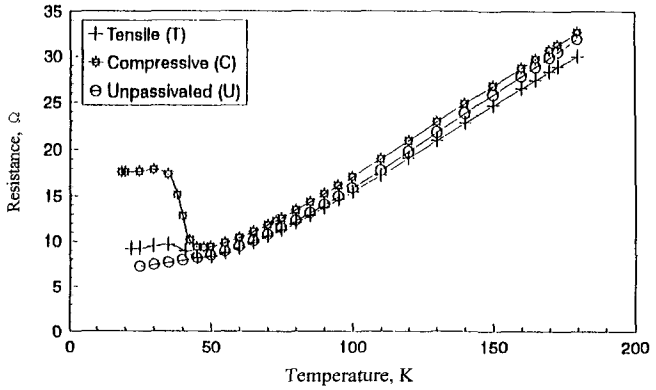

Fig. 3. R vs T for AlX interconnects with and without tensile and compressive ILDs.

reliability of AlX metallizations has been also proposed based on the above work [9, 10]. Its use in ULSIC manufacturing appears quite promising.

4. SUMMARY

It has been shown that the thermophysical properties of thin films, e.g., thermal conductivity, κ, and stress, σ, are important parameters which need to be understood and used in the IC process and layout design for enhanced performance and reliability in the current ULSICs and that they are even more important for the next generation ICs such as 3-D and UPICs. The κ of SiO_2 ILD films is lower than its value for bulk quartz, it decreases with decreasing film thickness, and it varies with the process used for its deposition. A quantitative technique to monitor the quality of the ILD films has been given which uses the extrapolated value of κ as an effective bulk quartz parameter for the process used for the ILD deposition. Further, a quantitative technique to monitor the adhesion of films has been given, which uses the slope s of the κ vs $1/t_{ox}^{1/2}$ straight line. The lowest value of s signifies the best adhesion. This technique is the only technique which allows monitoring of adhesion of films in submicron geometries used in ULSICs, during and after normal and accelerated electrical testing. It has been also shown that the stress of ILD films has an important effect on the reliability of ULSICs. A quantitative technique has been given to characterize and enhance the reliability of ULSICs by the measurement and monitoring of adhesion using electrical test structures.

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